



Attorney Docket No. YOR9-2000-0415 (8728-407)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Altman et al.

Serial No.: 09/637,078

Filed: August 11, 2000

For: METHOD AND APPARATUS FOR PROFILING
COMPUTER PROGRAM EXECUTION

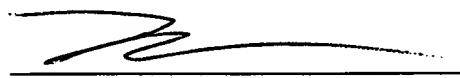
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1. Reply Brief
2. Return Postcard

Dated: September 18, 2006


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PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Applicants: Altman et al.

Examiner: W. Wood

Serial No: 09/637,078

Group Art Unit: 2193

Filed: August 11, 2000

Docket: YOR9-2000-0415 (8728-407)

For: **METHOD AND APPARATUS FOR PROFILING COMPUTER
PROGRAM EXECUTION**

REPLY BRIEF

This is a Reply to the Examiner's Answer mailed on July 17, 2006.

Appeal from Group 2193

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Appellants' Response to the Examiner's Response

Appellants maintain the previous arguments from the Appeal Brief mailed on April 10, 2006. In addition, Appellants wish to address the following issues raised by the Examiner in the Examiner's Response.

On page 26 of the Examiner's response, the Examiner states the following:

Krishnaswamy under the broadest reasonable interpretation does disclose "storing, in a memory array, profile counts ... the memory array being separate and distinct from the memory hierarchy" (column 5, line 35-45, column 6, lines 34-36 and figure 2, elements 70, 100, 110, 160, and 170; at least one interpretation is the profile information being stored in the elements 90 being separate and distinct from elements 70, 170, and 160).

It is respectfully submitted that Examiner's characterization of the teachings of Krishnaswamy in this regard is misplaced. Krishnaswamy teaches (in col. 4, lines 27-28) that an element 90 is known as a performance monitoring unit (PMU). However, a PMU 90 consists of multiple counters (as taught in col. 6, line 24 of Krishnaswamy) and is not a memory array. As essentially stated before in the supplemental argument mailed by Applicants on May 6, 2005, a counter is typically built with latches or flip flops, which are clocked elements, as differentiated from a memory. As further stated in the supplemental argument, counters are further differentiated from memory arrays in that counters cannot be addressed.

In addition, Krishnaswamy teaches that a PMU 90 is not a memory array. Krishnaswamy teaches (in col. 4, 24-28) that the PMU 90 includes multiple counters programmable to count events and (in col. 32-26) a dynamic optimization helper 230 (in shared user space, as taught by Figure 3) that periodically reads from the PMU counters to gather profile data to be stored to a log in shared user space (which is part of the memory hierarchy). If the PMU 90 functioned as a memory array separate and distinct from the

memory hierarchy, the step of periodically reading from the PMU counters so profile data can be stored elsewhere would be unnecessary.

On page 27 of the Examiner's response, the Examiner states the following:

Now continuing with Appellant's broad definition of memory hierarchy found in the brief, it becomes clear Appellant's cited definition would necessarily include the profile matrix as the definition necessarily includes registers and caches. Appellants originally filed disclosure states, an optimized profile matrix may consist of profile matrices (e.g., similar to caching hierarchies).

The definition cited by Appellants means only that many different types of memory elements (e.g., registers, cache, main memory, secondary storage (disks), offline storage(tapes) can be included within the memory hierarchy. To be clearer, a memory hierarchy is a hierarchical ordering and arrangement of a chosen subset of these memory elements into a collective body known as the memory hierarchy. Further, a statement that profile matrices may be similar to caching hierarchies does not necessarily mean that a profile matrix must be a cache. The organization of the matrices that may be similar to the organization of caches in a caching hierarchy. Further, when Krishnaswamy disclosed a main memory (memory 70), disk storage (permanent storage 160), and offline disk storage (removable media unit 170), it is assumed that these elements are part of the memory hierarchy since they are memory elements typically found in a memory hierarchy and Krishnaswamy never explicitly stated that they were separate from the memory hierarchy.

Conclusion

The Examiner has failed to establish a *prima facie* case of anticipation of the presently claimed invention under 35 U.S.C. § 102(e) over Krishnaswamy for at least the reasons noted above and in the Appeal Brief mailed on April 10, 2006. In addition, the

Examiner has failed to establish a *prima facie* case of obviousness of the presently claimed invention under 35 U.S.C. § 103(a) over the cited prior art for at least the reasons noted in the Appeal Brief. Accordingly, it is respectfully requested that the Board reverse the rejections under 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a).

Respectfully submitted,

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